



Device/PLC Connection Manuals



About the Device/PLC Connection Manuals

Prior to reading these manuals and setting up your device, be sure to read the "Important: Prior to reading the Device/PLC Connection manual" information. Also, be sure to download the "Preface for Trademark Rights, List of Units Supported, How to Read Manuals and Documentation Conventions" PDF file. Furthermore, be sure to keep all manual-related data in a safe, easy-to-find location.

5.1 Mitsubishi Electric

5.1.1 System Structure

The following describes the system structure for connecting the GP to Mitsubishi Electric PLCs.

YReference

The Cable Diagrams mentioned in the following tables are listed in the section titled "5.1.2 Cable Diagrams".

■ MELSEC-A Series (using Link I/F)

CPU	Link I/F	Cable Diagram	GP
	Computer Link Unit		
A2A	AJ71C24-S6	(Cable Diagram 1)	
A3A	AJ71C24-S8		
A4U	AJ71UC24		GP series
A2US	A1SJ71C24-R4		
	A1SJ71UC24-R4		
A2USH-S1	A1SJ71UC24-R4		

■ MELSEC-N Series (Link I/F)

CPU	Link I/F	Cable Diagram	GP
	Computer Link Unit	←	
A1N	AJ71C24		
A2N	AJ71C24-S3		
A3N	AJ71C24-S6		
	AJ71C24-S8		
	AJ71UC24	(Cable Diagram 1)	GP series
A0J2,A0J2H	A0J2-C214-S1		
A1S	A1SJ71C24-R4		
A1SJ,A2SH,A1SH	A1SJ71UC24-R4		
A2CCPU24	Link I/F on CPU unit		

■ MELSEC-FX Series (Expansion Board with Link I/F protocol)*1

CPU	Adapter	Cable Diagram	GP
	Expansion	•	
FX2N *2	FX2N-485-BD	RS-422 (Cable Diagram 2)	GP series

^{*1} Choose Mitsubishi's MELSEC-FX2(Link) as the GP-PRO/PBIII project file's PLC type.

■ MELSEC-OnA Series (using Link I/F)

CPU	Link I/F	Cable Diagram	GP
	Serial Communication Unit / Computer Link Unit	•	
Q2A,Q2A-S1,Q4A	AJ71QC24 (serial communication unit) *1 AJ71UC24 (computer link unit)	RS-422 (Cable Diagram 1)	
	AJ71QC24N-R4	RS-422	
		(Cable Diagram 2) for CN-1	
Q2AS	A1SJ71QC24N(serial	RS-422	
	communication unit) *2	(Cable Diagram 1)	GP series
	A1SJ71UC24(computer link		
	unit)		
Q2AS-S1	A1SJ71QC24N	RS-422	
	A1SJ71UC24-R4	(Cable Diagram 1)	
Q4AR	AJ71QC24N	RS-422	
		(Cable Diagram1)	

*1 ROM: must be higher than 7179B.

*2 ROM: must be higher than 7179M.

^{*2} The PLC's system version should be at least 1.06 or later. Check the PLC's version by reading out the data from the register (D8001). For detailed information refer to the Mitsubishi's FX 2N Series Micro Sequencer manuals.

■ MELSEC-Q Series

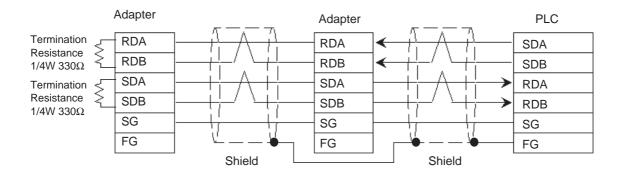
СРИ	Link I/F	Cable Diagram	GP
	Serial Communication Unit / Computer Link Unit		
Q02CPU-A	A1SJ71UC24-R4	RS-422	
Q02HCPU-A		(Cable Diagram 1)	
Q06HCPU-A	0.174.0.04	DO 100	
Q02C PU	QJ71C24	RS-422	
Q02HCPU		(Cable Diagram 1)	
Q06HCPU			GP series
Q12HCPU			
Q25HCPU			
Q00CPU			
Q01CPU			
C00JCPU			

5.1.2 Cable Diagrams

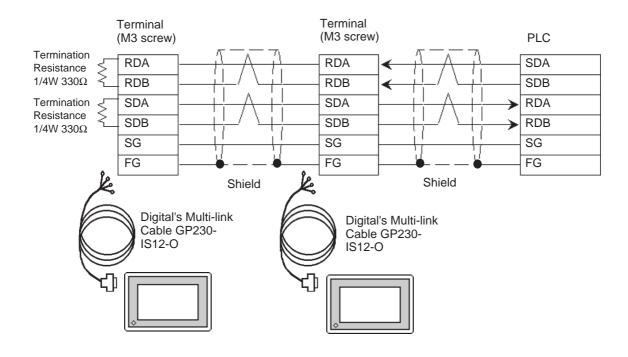
The cable doagrams illustrated below and the cable diagrams recommended by Mitsubishi Electric Corp. may differ, however, using these cables for your PLC operations will not cause any problems.

Cable Diagram 1

• When using Digital's RS-422 connector terminal adapter GP070-CN10-O



• When using Digital's Multi-link Cable, GP230-IS12-O





Ground your PLC's FG terminal according to your country's applicable standard. For details, refer to the corresponding PLC manual.



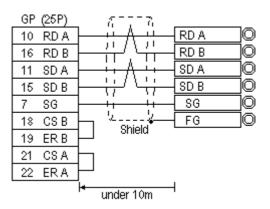
- Pull out the Transfer Cable Shield cover and shape it into a wire and connect it to the PLC's FG terminal.
- GP230-IS12-O Cable FG terminal is not connected to GP's FG.
- Place a Termination Resistor at both ends of the cable. The Termination Resistor is automatically setup when the PLC's Termination Resistor switch is turned ON.
- Fot the RS-422 connection, use a cable length less than 500m.
- As a general rule, connect the PLC at either end of the circuit, not in the middle.





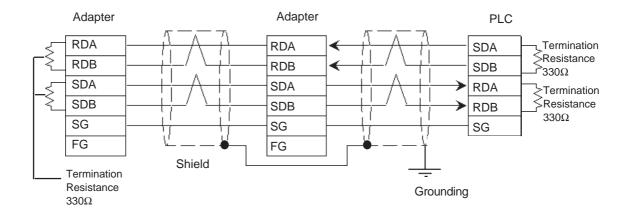
When making your own cable, Mitsubishi's SPEV (SB)-MPC-0.2*3P cable is recommended as the connection cable.

The cable connection lines are as illustrated below and should be less than 10m.

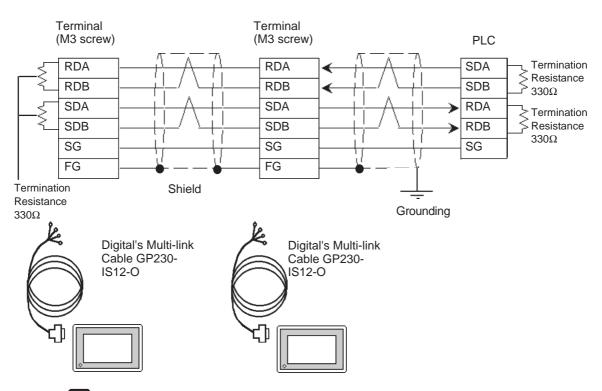


Cable Diagram 2

• When using Digital's RS-422 connector terminal adapter GP070-CN10-O



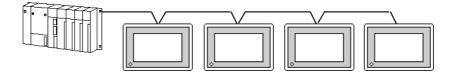
• When using Digital's GP230-IS12-0 (Multi Link Cable)



Ground your PLC's FG terminal according to your country's applicable standard. For details refer to your PLC's manual.

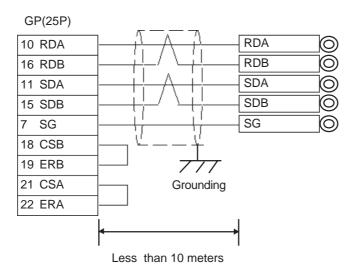


- Pull out a small amount of the Transfer Cable's shield, make a wire out of it and connect it to the PLC's FG terminal.
- The GP230-IS12-0 cable's FG terminal is not connected to the GP's FG line.
- Connect a terminating resistor to both ends of the cable.
- When using FX2N-485-BD, the cable must not be longer than 50m.
- As a general rule, connect the PLC at the end of the circuit's wiring (see below).





- When making your own cable, the Mitsubishi SPEV (SB)-MPC-0.2x3P is recommended.
- The cable connection lines are as shown below. The cables used between the GP and the terminals should be less than 10meters long.



5.1.3 Supported Devices

The following describes the range of devices supported by the GP.

■ MELSEC-A Series (AnA/ AnU/ A2US/ A2USH-S1)

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X1FFF	X0000 ~ X1FF0	<u>xx</u> 01	
Output Relay	Y0000 ~ Y1FFF	Y0000 ~ Y1FF0	[xxxO]	
Internal Relay	M0000 ~ M8191	M0000 ~ M8176	<u> </u>	
Latch Relay	L0000 ~ L8191	L0000 ~ L8176	<u> </u>	
Special Relay	M9000 ~ M9255	M9000 ~ M9240	<u>÷16</u> 1	
Annuniciator	F0000 ~ F2047	F0000 ~ F2032	<u>÷16</u> 1	
Link Relay	B0000 ~ B1FFF			
Timer (contact)	TS0000 ~ TS2047			
Timer (coil)	TC 0000 ~ TC 2047			L/H
Counter (contact)	CS0000 ~ CS1023			
Counter (coil)	CC0000 ~ CC1023			
Timer (current value)		TN 0000 ~ TN 2047		
Counter (current value)		CN0000 ~ CN1023		
Data Register		D0000 ~ D8191	Bit 1 51	
Special Register		D9000 ~ D9255	Bit 1 5 1	
Link Register		W0000 ~ W1FFF	Bit F	
File Register		R0000 ~ R8191	Bit 5] *1	

^{* 1} When using the File Register and the AnA or AnU, use the User's memory area in the memory cassettes.

When the File Register is setup when the memory cassette is not in use, an error will develop when communicating.

■ MELSEC-N Series (AnN/ A2C/ A1S/ A1SJ/A2SH)

Setup System Area or Communication Information's Storing Address here.

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X07FF	X0000 ~ X07F0	[XXXO]	
Output Relay	Y0000 ~ Y07FF	Y0000 ~ Y07F0	<u>xxx</u> O) *1	
Internal Relay	M0000 ~ M2047	M0000 ~ M2032	<u>÷16</u>	
Latch Relay	L0000 ~ L2047			
Special Relay	M9000 ~ M9255	M9000 ~ M9240	<u>÷</u> 161 *2	
Annuniciator	F0000 ~ F255	F000 ~ F240	<u>÷16</u>	
Link Relay	B0000 ~ B03FF			
Timer (contact)	TS000 ~ TS255		1 ,	L/H
Timer (coil)	TC000 ~ TC255			L/11
Counter (contact)	CS000 ~ CS255			
Counter (coil)	CC000 ~ CC255			
Timer (current value)		TN000 ~ TN255		
Counter (current value)		CN000 ~ CN255		
Data Register		D0000 ~ D1023	Bit 1 51	
Link Register		W0000 ~ W03FF	Bit F	
File Register		R0000 ~ R8191	Bit 1 5 1 *3	

^{* 1} The Output Relays Y01F0-Y01FF (word Y01F0) are used by the PLC, and cannot be set.. (only for A2C)

When the File Register is setup when the memory cassette is not in use, an error will develop when communicating.

^{* 2} A MELSEC-AnN and AJ71C24-S3 (or AJ71C24) cannot be matched and used.

^{* 3} When using the File Register and the AnN, use the User's memory area in the memory cassettes.

■ MELSEC-FX Series (using Expansion board with Link Protocol)

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X0267	X0000 ~ X0240	<u>ост</u> 8) [*** 0]	
Output Relay	Y0000 ~ Y0267	Y0000 ~ Y0240	ост 8] [*** 0]	
Auxiliary Relay	M0000 ~ M3071	M0000 ~ M3056	<u>÷ 16</u>)	
State	S0000 ~ S0991	S0000 ~ S0976	<u>÷ 16</u>)	
Special Auxiliary Relay	M8000 ~ M8255	M8000 ~ M8240	<u>÷ 16</u>) *1	
Timer (contact)	TS000 ~ TS255			L/H
Counter (contact)	CS000 ~ CS255			
Timer (current value)		TN 000 ~ TN 255		
Counter (current value)		CN000 ~ CN255	*2	
Data Register		D0000 ~ D7999	<u>ві т</u> 15)	
Special Data Register		D8000 ~ D8255	<u>ві т</u> 15) *1	

^{*1} The Special Relay and the Special Data Register are divided into three areas. These are the Exclusive Reading Area, the Exclusive Writing Area and the System Area. For details, refer to your PLC's manual.

^{*2} Word addresses CN200 to CN255 are 32 bit counters.

■ MELSEC-QnA Series

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X1FFF	X0000 ~ X1FF0	*** 0	
Output Relay	Y0000 ~ Y1FFF	Y0000 ~ Y1FF0	*** 0	
Internal Relay	M00000 ~ M32767	M00000 ~ M32752	<u>÷16</u> 1	
Special Relay	SM0000 ~ SM2047	SM0000 ~ SM2032	<u>÷16</u>)	
Latch Relay	L00000 ~ L32767	L00000 ~ L32752	÷16)	
Annunciator	F00000 ~ F32767	F00000 ~ F32752	<u>÷16</u>)	
Edge Relay	V00000 ~ V32767	V00000 ~ V32752	<u>÷16</u>)	
Step Relay	S0000 ~ S8191	S0000 ~ S8176	<u>÷16</u>)	
Link Relay	B0000 ~ B7FFF	B0000 ~ B7FF0	*** 0	
Special Relay	SB000 ~ SB7FF	SB000 ~ SB7F0	*** 0	
Timer (contact)	TS00000 ~ TS22527			
Timer (coil)	TC00000 ~ TC22527			
Aggregation Timer (contact)	SS00000 ~ SS22527			L/H
Aggregation Timer (coil)	SC00000 ~ SC22527			
Counter (contact)	CS00000 ~ CS22527			
Counter (coil)	CC00000 ~ CC22527			
Timer (current value)		TN00000 ~ TN22527		
Aggregation Timer (current value)		SN00000 ~ SN22527		
Counter (current value)		CN00000 ~ CN22527		
Data Register		D00000 ~ D25599	<u>в і т</u> 15	
Special Register		SD0000 ~ SD2047	Bit F	
Link Register		W0000 ~ W63FF	B i t F	
Special Link Register		SW000 ~ SW7FF	<u>в і т</u> 15)	
File Register (nomal)		R00000 ~ R32767	_{Ві t} 15] *1	
File Register (serial)		0R0000 ~ 0R7FFF 1R0000 ~ 1R7FFF	<u>B i t</u> F] *1	

^{* 1} When using the File Register, a Memory Card is necessary. Depending on the Memory Card being used, the File Register's device range differs.

■ MELSEC-Q Series (A Mode CPU)

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X1FFF	X0000 ~ X1FF0	*** 0]	
Output Relay	Y0000 ~ Y1FFF	Y0000 ~ Y1FF0	* * * 0]	
Internal Relay	M0000 ~ M8191	M0000 ~ M8176	<u>÷16</u>)	
Latch Relay	L0000 ~ L8191	L0000 ~ L8176	<u>÷16</u>)	
Special Relay	M 9000 ~ M 9255	M9000 ~ M9240	<u>÷16</u>)	
Annunciator	F0000 ~ F2047	F0000 ~ F2032	<u>÷16</u> j	
Link Relay	B0000 ~ B1FFF			
Timer (Contact)	TS0000 ~ TS2047			
Timer (Coil)	TC0000 ~ TC2047			L/H
Counter (Contact)	CS0000 ~ CS1023			
Counter (Coil)	CC0000 ~ CC1023			
Timer (Current Value)		TN0000 ~ TN2047		
Counter (Current Value)		CN0000 ~ CN1023		
Data Register		D0000 ~ D8191	B i t 15]	
Spcial Register		D9000 ~ D9255	B i t 15]	
Link Register		W0000 ~ W1FFF	Bit F	
File Register		R0000 ~ R8191	B i t 15 *1	_

^{* 1} The amount of space available when using the File Register will vary, depending on the amount of CPU ROM/RAM available, or the amount of memory available on the memory card.

■ MELSEC-Q Series (Q Mode CPU)

Setup System Area or Communication Information's Storing Address here.

Device	Bit Address	Word Address	Particulars	
Input Relay	X0000 ~ X1FFF	X0000 ~ X1FF0	*** 0	
Output Relay	Y0000 ~ Y1FFF	Y0000 ~ Y1FF0	***0	
Internal Relay	M00000 ~ M32767	M00000 ~ M32752	<u>÷16</u>)	
Special Relay	SM0000 ~ SM2047	SM0000 ~ SM2032	<u>÷16</u>)	
Latch Relay	L00000 ~ L32767	L00000 ~ L32752	<u>÷16</u>)	
Annunciator	F00000 ~ F32767	F00000 ~ F32752	<u>÷16</u>)	
Edge Relay	V00000 ~ V32767	V00000 ~ V32752	<u>÷16</u>)	
Step Relay	S0000 ~ S8191	S0000 ~ S8176	<u>÷16</u>)	
Link Relay	B0000 ~ B7FFF	B0000 ~ B7FF0	*** 0	
Special Relay	SB000 ~ SB7FF	SB000 ~ SB7F0	*** 0	
Timer (contact)	TS00000 ~ TS23087			
Timer (coil)	TC00000 ~ TC23087			
Aggregation Timer (contact)	SS00000 ~ SS23087			L/H
Aggregation Timer (coil)	SC00000 ~ SC23087			
Counter (contact)	CS00000 ~ CS23087			
Counter (coil)	CC00000 ~ CC23087			
Timer (current value)		TN00000 ~ TN23087		
Aggregation Timer (current value)		SN00000 ~ SN23087		
Counter (current value)		CN00000 ~ CN23087		
Data Register		D00000 ~ D25983	_{В і т} 15)	
Special Register		SD0000 ~ SD2047	B i t 15]	
Link Register		W0000 ~ W657F	Bit F)	
Special Link Register		SW000 ~ SW7FF	Bit F	
File Register (nomal)		R00000 ~ R32767	_{В і т} 15] *1	
		0R0000 ~ 0R7FFF	B i t F) *1	
File Register (serial)		1R0000 ~ 1R7FFF	B i t F) *1	
i ile regisier (serial)	:	:	:	
		31R0000 ~ 31R67FF	Bit F) *1	

^{* 1} The amount of space available when using the File Register will vary, depending on the amount of CPU ROM/RAM available, or the amount of memory available on the memory card.



• The device ranges given here are based on the maximum values possible for parameter settings. Depending on your CPU, usable device types and range may differ. Before using, refer to your CPU user manual.

5.1.4 Environment Setup

The following lists Digital's recommended PLC and GP communication settings.

■ MELSEC-A Series (When using Computer Link I/F)

G	iP Setup	PLC (Data Registe	r) Setup
Baud Rate	19200 bps	Baud Rate	19200
Data Length	7 bit	Data Length	7 bit
Stop Bit	2 bit	Stop Bit	2 bit
Parity Bit	Even	Parity Check Parity setting even/odd	Yes Even
Data Flow Control	ER Control		
Communication Format	4-wire type	C hannel setup	RS-422
		Mode Setup	8 (Format 4 protocol)
		Write during RUN	Yes
		Sumcheck	Yes
		Transmission area terminal resistance	Present
Receiving area terminal resistance		Present	
Unit No.	0	Station No.	0

\blacksquare MELSEC-FX Series (FX_{2N})

GP Setup		PLC (Data Register) Setup	
Baud Rate	19200 bps	Baud Rate	19200
Data Length	7	Data Length	7
Stop Bit	2	Stop Bit	2
Parity Bit	Even	Parity Bit	Even
Data Flow Control	ER Control		
Communication Format	4-wire type	Computer Link	RS485(RS422) I/F
Station No.	0	Station No.	0
		Sumcheck	Yes
		Protocol	Yes
		Mode	Format 4 protocol
		Header	No
		Terminator	No



• PLC's Station NO. data must be written in data register D8121 and other settings must be written in data register D8120. For details refer to Mitsubishi's "FX Communication Users Manual".

■ MELSEC-QnA Series

GP Setup		PLC (Data I	PLC (Data Register) Setup	
Baud Rate	19200 bps *1	Baud Rate	19200	
Data Length	7 bit	Data Length	7 bit	
Stop Bit	2 bit	Stop Bit	2 bit	
Parity Bit	Even	Parity Check Parity setting even/odd	Yes Even	
Data Flow Control	ER Control			
Communication Format	4-wire type	Mode Setup	4 (Format 4 protocol)	
		Sumcheck	Yes	
		Transmission area terminal resistance	Present	
		Receiving area terminal resistance	Present	
Unit No.	0	Station No.	0	

*1 AJ71QC24N-R4, A1SJ71QC24N, AJ71QC24N can use a baud rate of 115.2kbps.



- CH1 and CH2 of a serial communication unit can communicate at the same time, given any of the following conditions.
- Refer to the MELSEC A Series table when using environment with MELSEC QnA and Computer Link I/F AJ71UC24 together.

Condition 1: The sticker on the top of the communication unit indicates the version is AB or later.

Condition 2: The date shown on the side of the communication unit indicates it was produced in September 1996 (9609) or later.

Condition 3: The communication ROM version is 7179M or later.

■ MELSEC-Q Series (using A Mode CPU Computer Link Unit)

GP Setup		Computer Link Unit Settings	
Baud Rate	19200 bps (fix ed)	Baud Rate	19200 bps
Data Length	7 bits (fixed)	Data Length	7 bits
Stop Bit	2 bits (fix ed)	Stop Bit	2 bits
Parity Bit	Even	Parity Check Parity setting even/odd	Yes Even
Data Flow Control	ER Control		
Communication Format (RS-422)	4-wire type	Mode Setup (RS-422)	8 (Format 4 Protocol Mode)
		Write possible in RUN mode	Possible
		Sumcheck	Yes
Unit No.	0 (fix ed)	Station No.	0

■ MELSEC-Q Series (Q Mode CPU Serial Communication Unit)

GP Setup		Serial Communication Unit Settings *1	
Baud Rate	19200 bps	Baud Rate	19200 bps
Data Length	7 bits	Data Length	7 bits
Stop Bit	2 bits	Stop Bit	2 bits
Parity Bit	Even	Parity Check Parity setting even/odd	Yes Even
Data Flow Control	ER Control		
Communication Format (RS-422)	4-wire type	Mode Setup (RS-422)	4 (Format 4 Protocol Mode)
		Sumcheck	Yes
Unit No.	0	Station No.	0

^{*1} The setting is made by Mitsubishi's GPP function software.